NH2307

P-Channel Enhancement Mode Trench Power MOSFET

Pb-Free RoHS COMPLIANT

Voltage:	-30	Volts	**Current:**	-2.7	Amperes	**Package:**	SOT-23

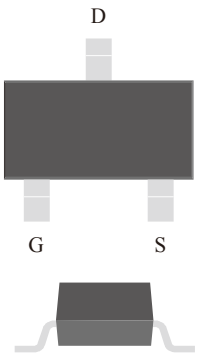
Features

- NH'S Advanced Trench Technology
- Low Rds(on) For Low On-State Loss
- High EAS For High Reliability
- Excellent Qg*Rds(on) Product(FOM）

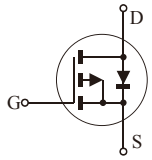
Typical Applications

- DC-DC Converter
- Battery Management System(BMS)
- Printed Circuit Board For Control Circuit
- Uninterrupible Power Supplies(UPS)

Diagram:



Polarity:



Product Summary

VDS Min.@T_j	-30	**V**
I_D Min.@Ta	-2.7	**A**
RDS(ON)(TYP)@-10V	73	**mΩ**

***100% UIS TESTED**

***100% ΔVDS TESTED**

Absolute Maximum Ratings (Ta=25℃ Unless Otherwise Specified)

Parameter	Test Conditions	Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (Note 1)	Ta= 25 ℃ Ta= 100 ℃	I_D	-2.7 -1.7	A
Drain Current-Pulse (Note 1)	T_J< 150 ℃	I_{DM}	-10.8	A
Maximum Power Dissipation Power Dissipation Derating Factor Above 25℃	Ta= 25 ℃ Ta= 100 ℃	P_D	1106 442	mW
Derating Factor		D_F	8.85	mW/℃

Thermal Characteristcs (Ta=25℃ Unless Otherwise Specified)

Parameter	Test Conditions	Symbol	Typ.	Unit
Junction Temperature		T_J	-55 to 150	℃
Storage Temperature Range		T_{STD}	-55 to 150	℃
Thermal Resistance Junction To Ambient With Steady-State	Still Air Environment With Ta=25℃	$R_{\theta JA}$	113	℃/W

Notes: 1.Pulse Width Limited By Max. Junction Temperature. (See Fig.14)

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Electrical Characteristcs (Ta=25℃ Unless Otherwise Specified)

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Static Off Characteristics						
Drain-Source Breakdown Voltage	VGS=0V,ID=250uA	BV_{DSS}	-30	--	--	V
Bvdss Temperature Coefficient	ID=250uA,Reference25℃	$\Delta BV_{DSS}/\Delta T_J$	--	0.03	--	V/℃
Drain-Source Leakage Current	VDS= -30 V,VGS=0V	I_{DSS}	--	--	-1	uA
Gate-Body Leakage Current	VGS= ±20 V,VDS=0V	I_{GSS}	--	--	±100	nA
Static On Characteristics						
Gate Threshold Voltage	VGS= VDS ID=-250uA	$V_{GS(TH)}$	-1	-1.5	-2.5	V
Drain-Source On Resistance	ID= -1.4 A,VGS= -10.0 V ID= -1.4 A,VGS= -5.0 V	$R_{DS(ON)}$	-- --	73 112	88 140	mΩ
Dynamic Characteristics						
Input Capacitance	VDS= -15 V VGS= 0 V F= 1 MHZ	C_{iss}	--	303	--	pF
Output Capacitance		C_{oss}	--	52	--	pF
Reverse Transfer Capacitance		C_{rss}	--	42	--	pF
Switching Paramters With Inductive Load(Test Circuit & Waveform See Fig.15)						
Turn-On Delay Time	VDS= -15 V VGS= -10.0 V RG= 10.0 Ω	$t_{d(on)}$	--	15	--	ns
Turn-On Rise Time		t_r	--	61	--	ns
Turn-Off Delay Time		$t_{d(off)}$	--	19	--	ns
Turn-Off Rise Time		t_f	--	10	--	ns
Gate Charge Paramters (Test Circuit & Waveform See Fig.16)						
Total Gate Charge	VDS= -15 V VGS= -10.0 V ID= -2.7 A	Q_g	--	8.1	--	nC
Gate-Source Charge		Q_{gs}	--	1.2	--	nC
Gate-Drain Charge		Q_{gd}	--	1.6	--	nC
Drain-Source Diode Characteristics And Maximum Ratings (Test Circuit & Waveform See Fig.18)						
Max. Diode Forward Current		I_S	--	--	-2.7	A
Max. Pulsed Forward Current		I_{SM}	--	--	-11	A
Diode Forward Voltage	ID= -1.4 A,VGS=0V	V_{SD}	--	-0.7	-1.2	V

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Typical Characteristics Curves

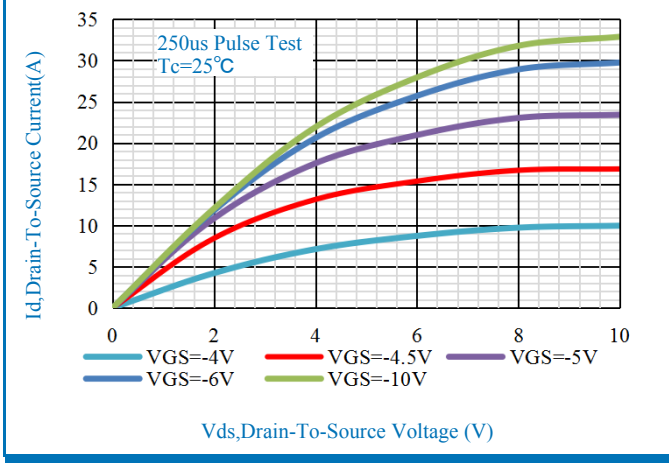


Fig.1-Output Characteristic

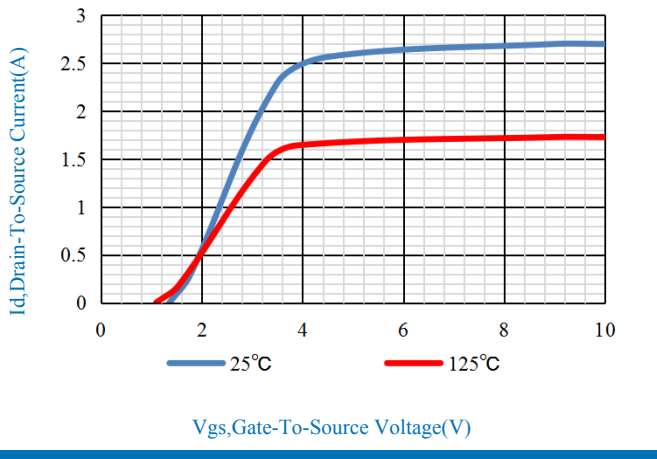


Fig.2-Transfer Characteristic

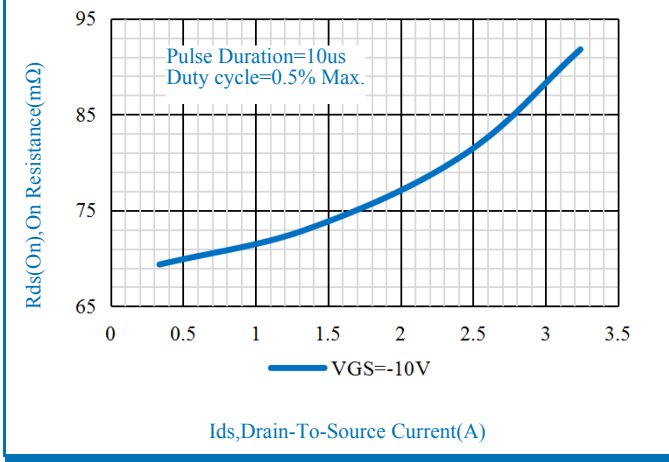


Fig.3-On Resistance Vs. Drain Current

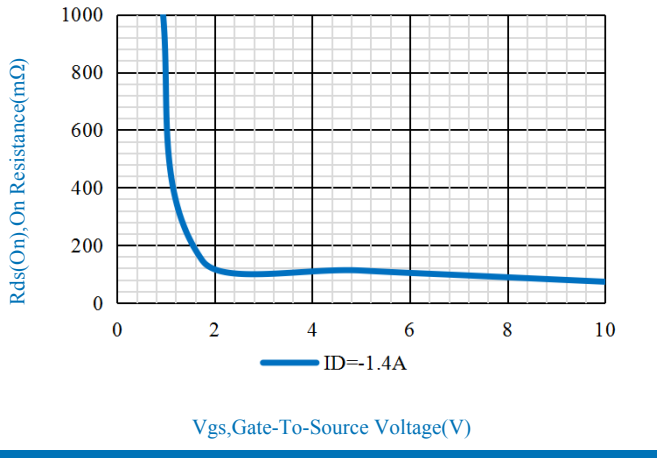


Fig.4-On Resistance Vs. Gate Source Voltage

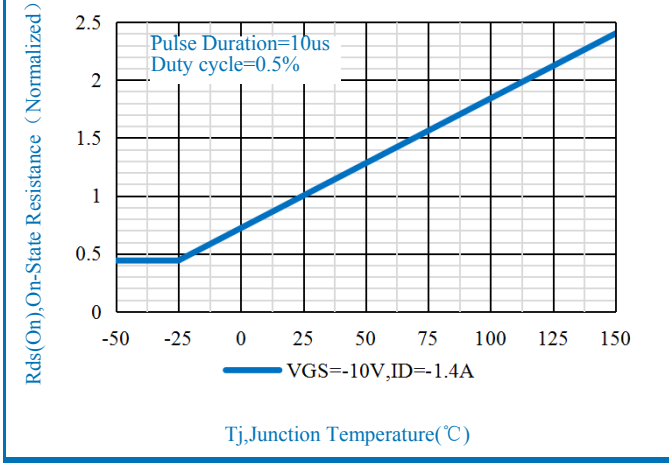


Fig.5-On Resistance Vs. Junction Temperature

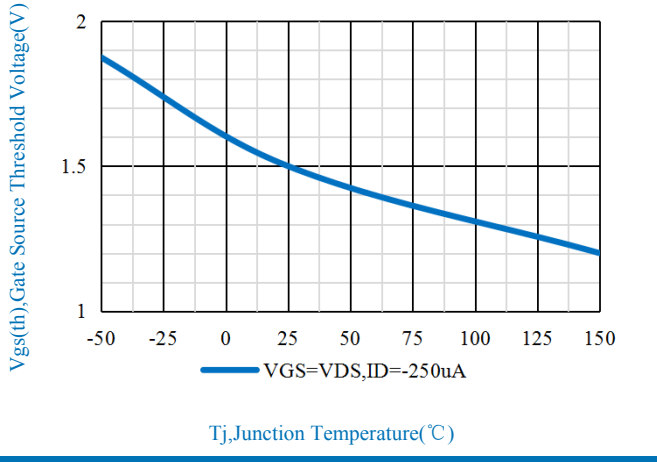


Fig.6-Gate Source Threshold Voltage Vs. Junction Temperature

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Typical Characteristics Curves

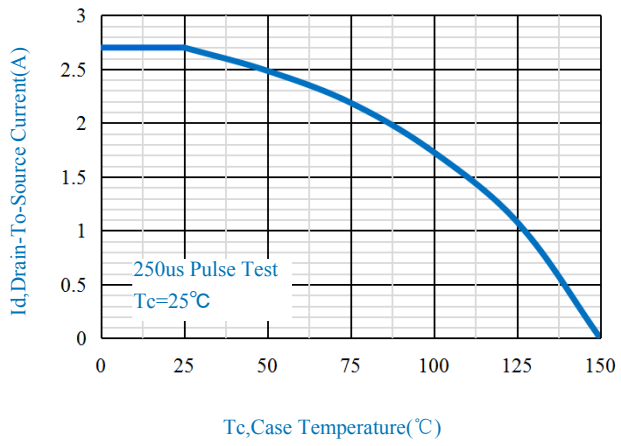


Fig.7-Maximum Continuous Drain Current Vs. Case Temperature

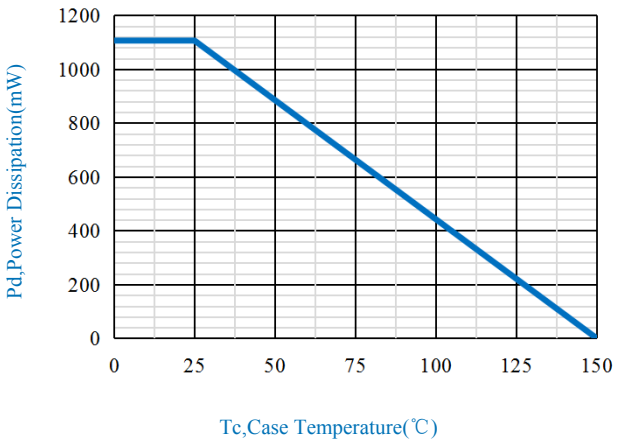


Fig.8-Maximum Power Dissipation Vs. Case Temperature

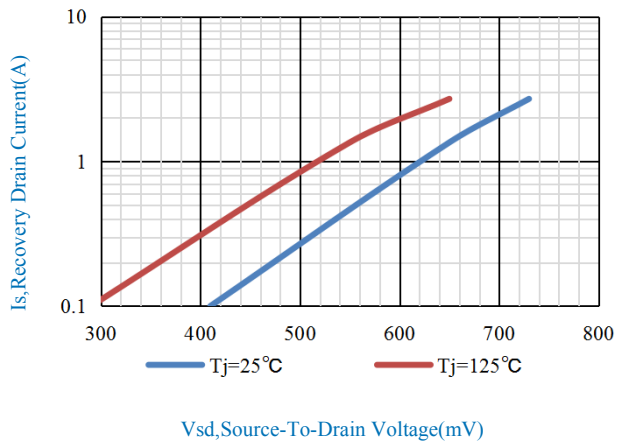


Fig.9-Source-To-Drain Diode Forward Voltage

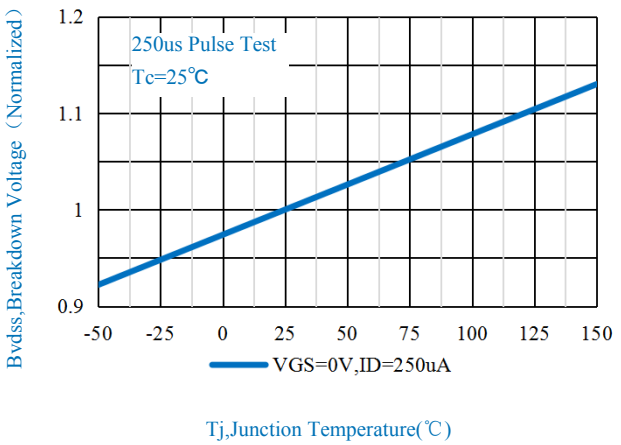


Fig.10-Breakdown Voltage Vs. Junction Temperature

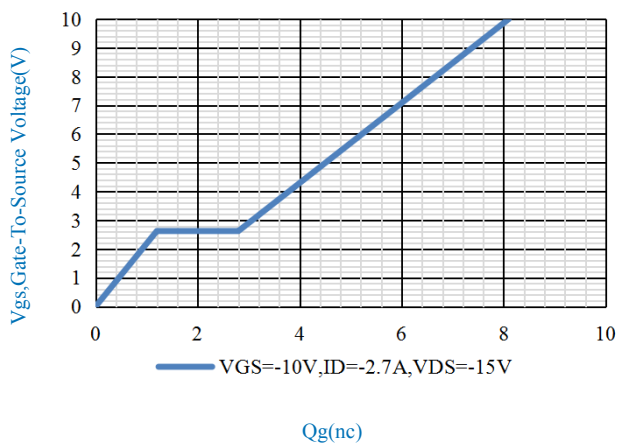


Fig.11-Gate Charge Waveform

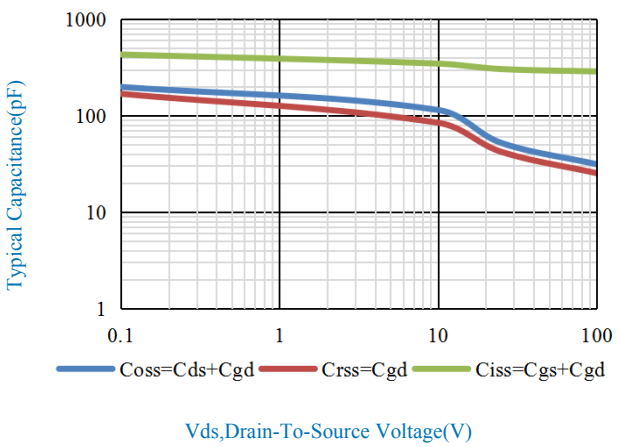


Fig.12-Typical Capacitance Vs. Drain-To-Source Voltage

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Typical Characteristics Curves

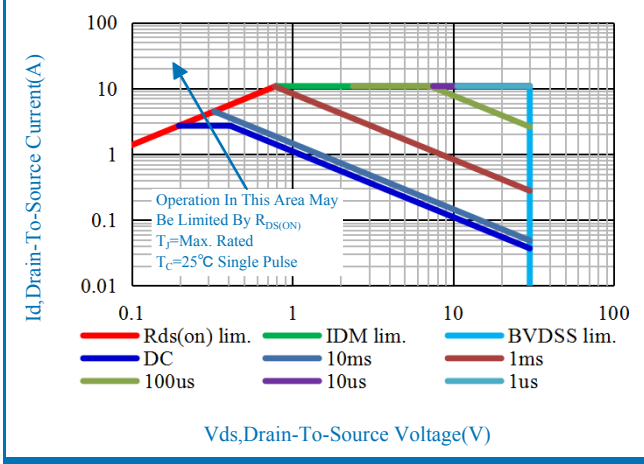


Fig.13-Maximum Safe Operating Area(SOA)

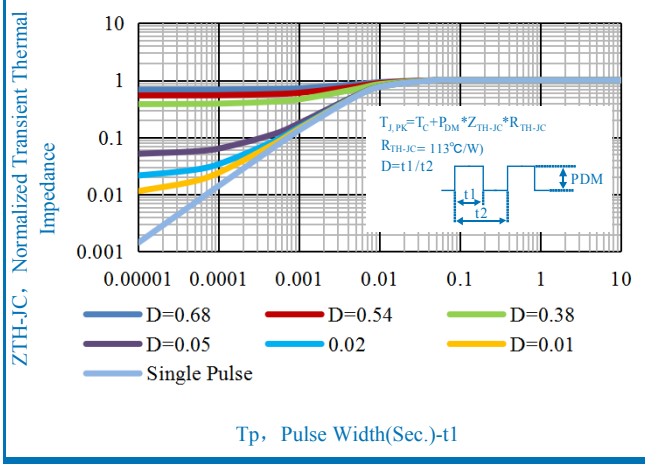
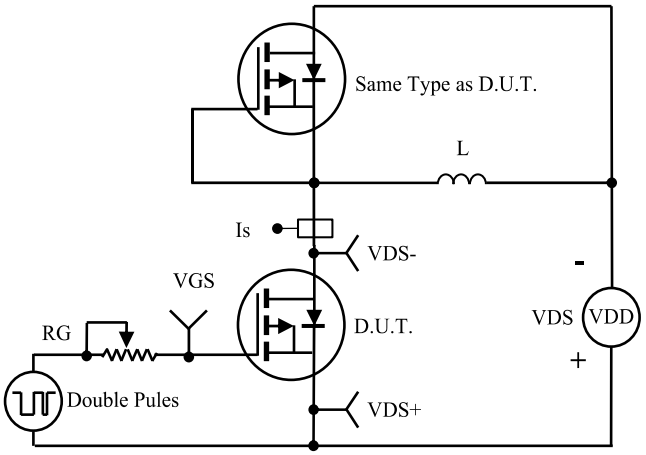


Fig.14- Normalized Maximum Transient Thermal Impedance Vs.Pulse Width

Inductive Load Test Circuit & Waveform



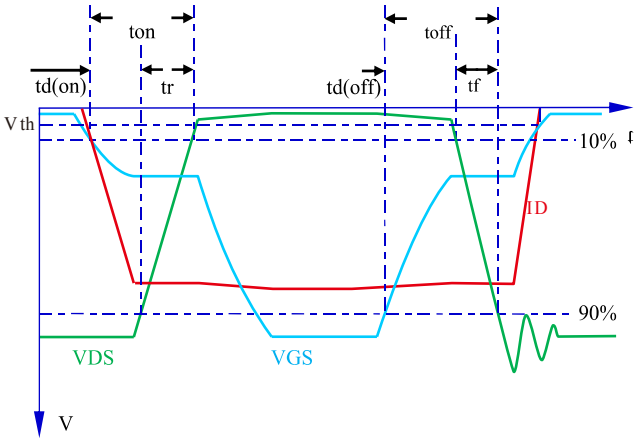


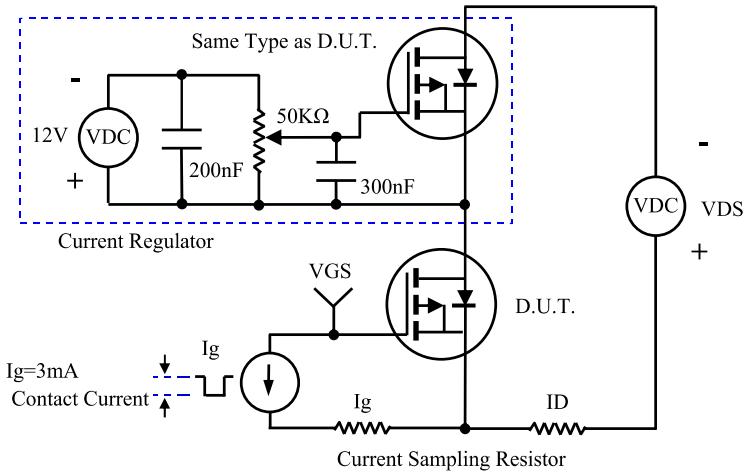
Fig.15- Inductive Switching Test Circuit & Waveform

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Test Circuit & Waveform



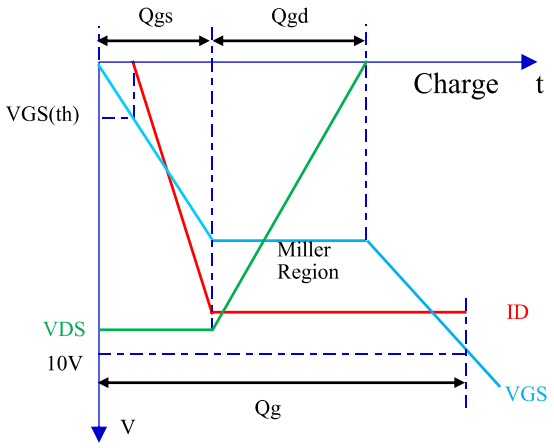
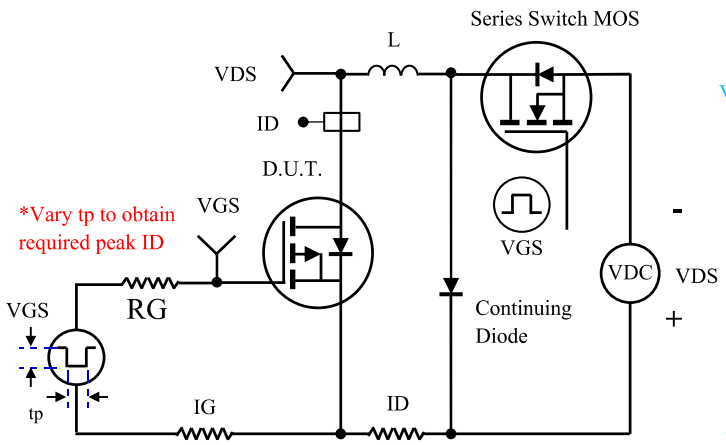


Fig.16-Gate Charge Test Circuit & Waveform



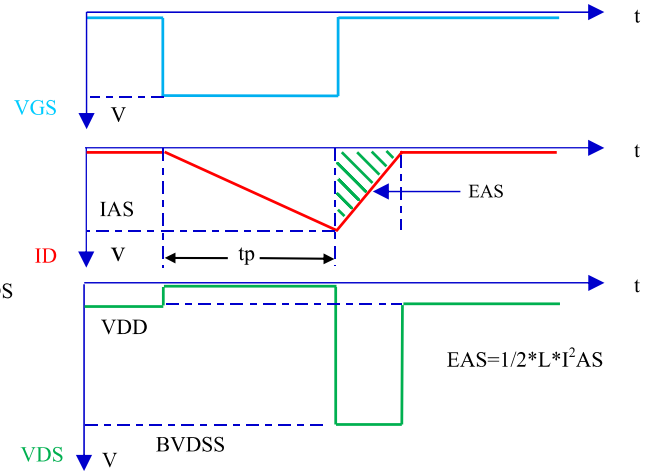
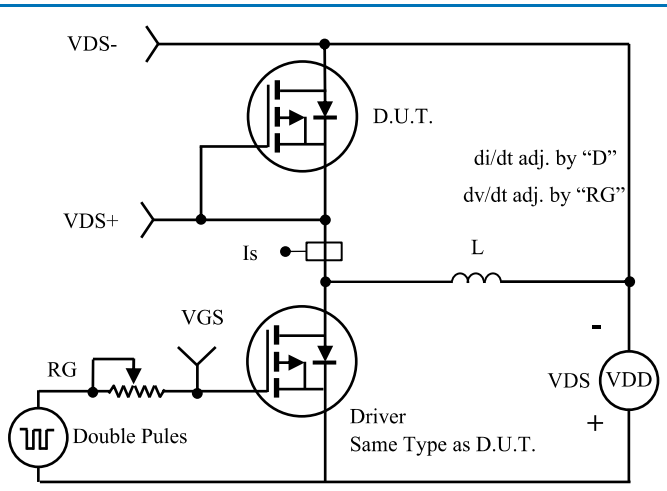


Fig.17- Unclamped Inductive Switching (UIS) Test Circuit & Waveform



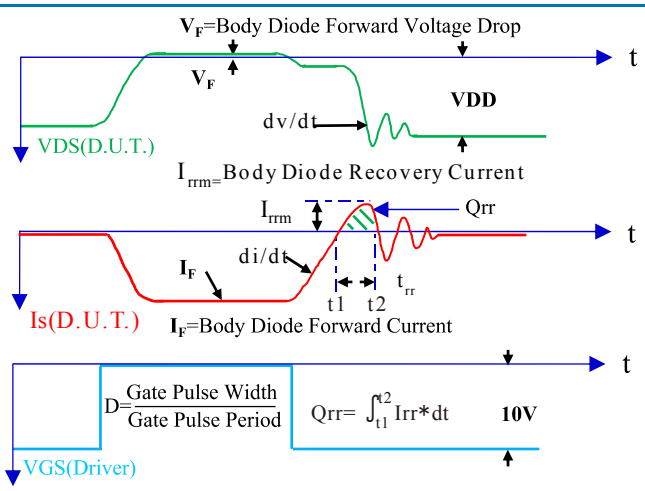


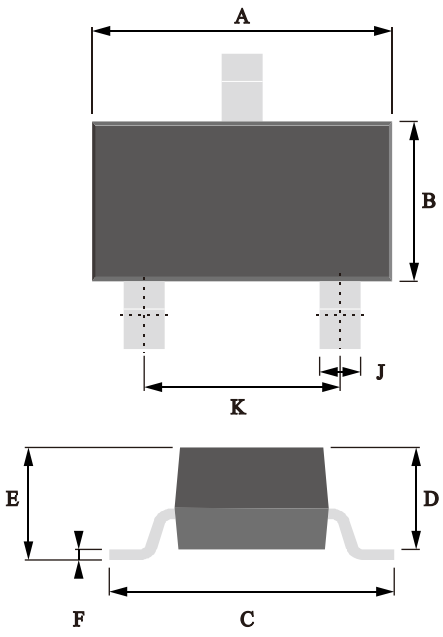
Fig.18- Diode Recovery Test Circuit & Waveform

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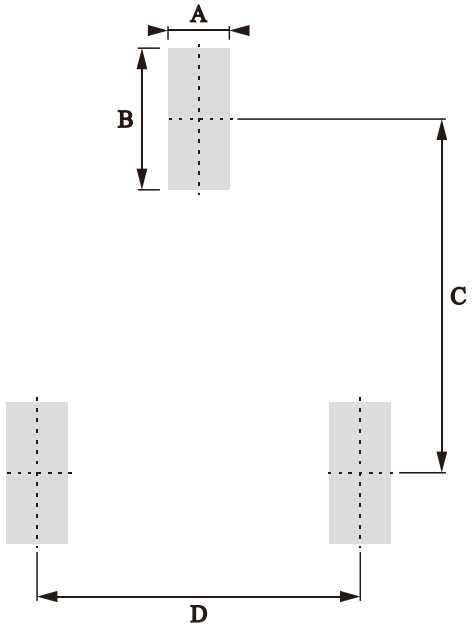
OUTLINE DRAWINGS



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OUTLINE DIMENSIONS						
Dim.	Milimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.80	-	3.20	0.1102	-	0.1260
B	1.15	-	1.45	0.0453	-	0.0571
C	2.25	-	2.65	0.0886	-	0.1043
D	0.85	-	1.15	0.0335	-	0.0453
E	0.90	-	1.20	0.0354	-	0.0472
F	0.08	-	0.18	0.0031	-	0.0071
J	0.30	-	0.50	0.0118	-	0.0197
K	1.70	-	2.10	0.0669	-	0.0827

RECOMMEDNED LAYOUT DRAWINGS



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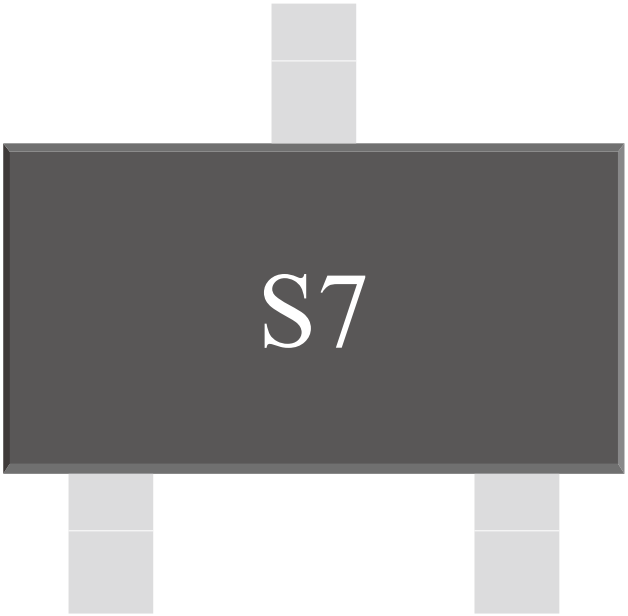
OUTLINE DIMENSIONS						
Dim.	Milimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	0.60	-	-	0.0000	-
B	-	0.80	-	-	0.0315	-
C	-	2.00	-	-	0.0787	-
D	-	1.90	-	-	0.0748	-

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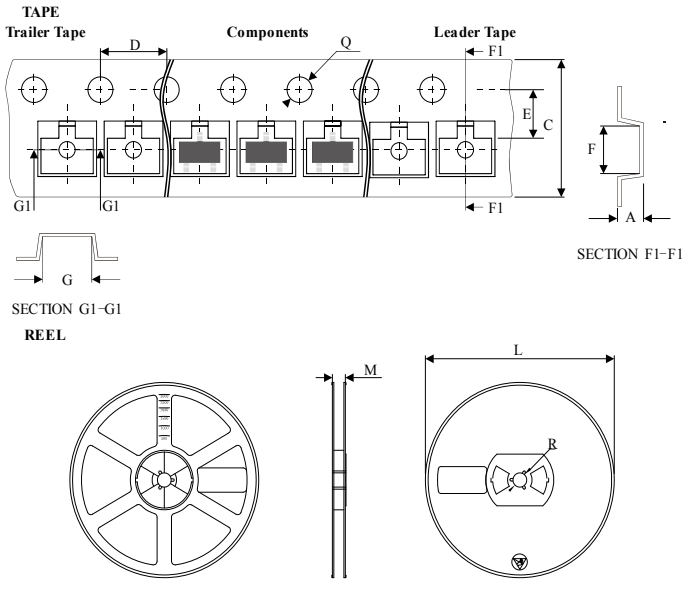
MARKING



MARKING INSTRUCTION

S7=MarK

PACKAGING



SOT-23

OUTLINE DIMENSIONS						
Dim.	Milimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
TAPE						
A	1.12	-	1.32	0.0441	-	0.0520
C	7.90	-	8.10	0.3110	-	0.3189
D	3.70	-	4.30	0.1457	-	0.1693
E	3.40	-	3.60	0.1339	-	0.1417
F	2.67	-	2.87	0.1051	-	0.1130
G	3.05	-	3.25	0.1201	-	0.1280
Q Φ	1.40	-	1.60	0.0551	-	0.0630
REEL						
L Φ	176.00	-	180.00	6.929	-	7.087
R	12.00	-	14.00	0.4724	-	0.5512
M	11.00	-	13.00	0.4331	-	0.5118

PACKING INFORMATION

Package Type	Package Code	Productor Weight Approx(g/Pcs)	Package Method	Quantity (Pcs/Min. Pack.)	Quantity (Pcs/Inner Box)	Quantity (Pcs/Carton)
SOT-23	P1	0.008	7" Reel	3000	45000	180000

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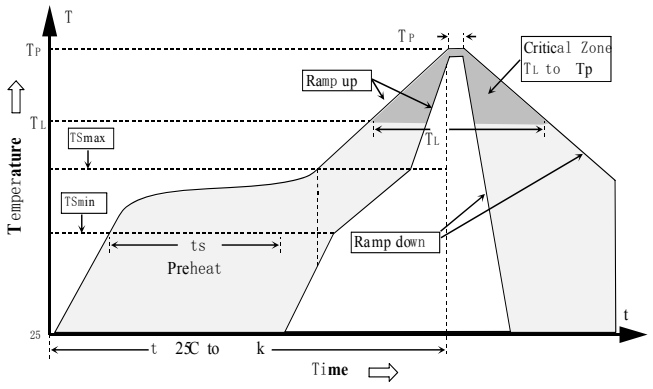
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Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat−Temperature Min (TS min) −Temperature Max (TS max) −Time(ts min to ts max)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: −Temperature (TL) − Time (tL)	183°C 60-150 seconds	217°C 60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature (tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

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- When the appearance of the product and chip size does not change, in order to product the customer. quality, change the internal structure and the production process Niuhang can not notify

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Specification Revision History

Rev.	Date	Changed Items	Pre-Changed Content	Changed Content
A/1	2014-10-20	First Issue		

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